BGS15M2A12

SP5T Diversity Antenna Switch with MIPI RFFE Interface

Data Sheet

Revision 3.0 - 2016-02-22

Power Management & Multimarket

Edition 2016-02-22

Published by Infineon Technologies AG
81726 Munich, Germany

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Document No.: BGS15M2A12__v3.0.pdf	
Revision History: Rev. v3.0	
Previous Version: 2.1	
Page	**Subjects (major changes since last revision)**
9	IL/RL/ISO/H2/H3 limits updated in Table 6
16	Marking layout updated in Figure 6
16	Carrier tape drawing updated in Figure 7

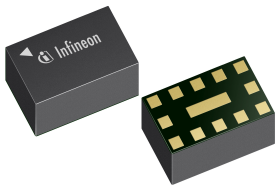
Contents

List of Figures

List of Tables

BGS15M2A12 SP5T Diversity Antenna Switch with MIPI RFFE Interface

1 Features



- Suitable for multi-mode LTE / WCDMA diversity Applications
- Ultra-low insertion loss and harmonics generation
- 5 high-linearity, interchangeable RX ports
- 0.1 to 2.7 GHz coverage
- High port-to-port-isolation
- No decoupling capacitors required if no DC applied on RF lines
- Integrated MIPI RFFE interface operating in 1.1 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- Small form factor 1.1 mm x 1.9 mm
- No power supply blocking required
- High EMI robustness
- RoHS and WEEE compliant package

RoHS

2 Product Description

The BGS15M2A12 RF MOS switch is specifically designed for LTE and WCDMA diversity applications. This SP5T offers low insertion loss and low harmonic generation.

The switch is controlled via a MIPI RFFE controller. The on-chip controller allows power-supply voltages from 1.1 to 1.95 V. Unlike GaAs technology, external DC blocking capacitors at the RF Ports are only required if DC voltage is applied externally. The BGS15M2A12 RF Switch is manufactured in Infineon's patented MOS technology, offering the performance of GaAs with the economy and integration of conventional CMOS including the inherent higher ESD robustness. The device has a very small size of only 1.1 x 1.9 mm^2 and a maximum height of 0.65 mm.

Table 1: Ordering Information

Type	Package	Marking
BGS15M2A12	ATSLP-12-5	55

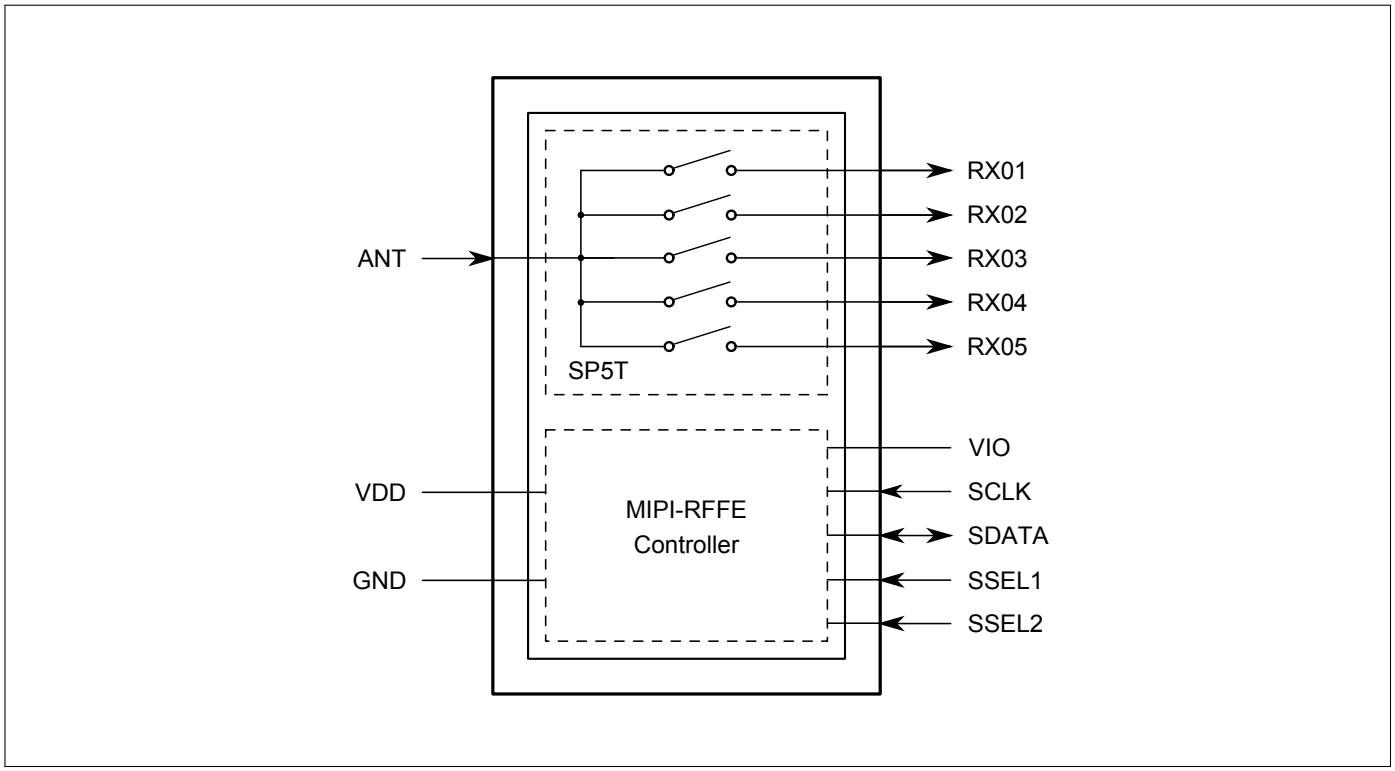


Figure 1: BGS15M2A12 Block diagram

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.1	–	–	GHz	[1]
Supply voltage	V_{DD}	-0.5	–	3.6	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–
RF input power at all Rx ports	P_{RF_Rx}	–	–	32	dBm	CW
ESD capability, HBM[3]	V_{ESD_HBM}	-1	–	+1	kV	Digital, digital versus RF
		-1	–	+1	kV	RF
ESD capability, system level[4]	V_{ESD_ANT}	-8	–	+8	kV	ANT versus system GND, with 27 nH shunt inductor

[1] There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0V.
[3] Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R=1.5 kΩ, C=100 pF).
[4] IEC 61000-4-2 (R=330 Ω, C=150 pF), contact discharge.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
RFFE Supply Voltage	V_{IO}	-0.5	–	3.6	V	–
RFFE Control Voltage Levels	V_{SCLK}, V_{SDATA}	-0.7	–	V_{IO}+0.7 (max. 3.6)	V	–

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.6	–	3.4	V	–
Supply current[2)]	I_{DD}	–	75	200	µA	–
Supply current in standby mode[2)]	I_{DD}	–	0.5	1	µA	VIO=low or MIPI low-power mode
RFFE supply voltage	V_{IO}	1.1	1.8	1.95	V	–
RFFE input high voltage[1)]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1)]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1)]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1)]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	15	–	µA	Idle State
Ambient temperature	T_A	-30	25	85	°C	–

[1)] SCLK and SDATA
[2)] T_A = –30 °C ... 85 °C, V_{DD} = 1.6 ... 3.4 V

Table 5: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rx ports (50 Ω)	P_{RF_Rx}	–	–	28	dBm	–

5 RF Characteristics

Table 6: RF Characteristics at T_A = –30 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{DD}= 1.6 V...3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1]						
All Rx Ports	IL	–	0.30	0.40	dB	100 to 1000MHz
		–	0.35	0.50	dB	1000 to 2000MHz
		–	0.40	0.55	dB	2000 to 2700MHz
		–	0.55	0.75	dB	2700 to 3800MHz
Return Loss[1]						
All Rx Ports	RL	25	31	–	dB	100 to 1000MHz
		22	28	–	dB	1000 to 2000MHz
		20	26	–	dB	2000 to 2700MHz
		14	20	–	dB	2700 to 3800MHz
Isolation[1]						
All Rx Ports	ISO	28	38	–	dB	100 to 1000MHz
		23	34	–	dB	1000 to 2000MHz
		20	30	–	dB	2000 to 2700MHz
		18	27	–	dB	2700 to 3800MHz
Harmonic Generation (UMTS Band 1, Band 5)[1]						
2^{nd} harmonic generation	P_{H2}	–	-100	-95	dBc	25 dBm, 50 Ω, CW mode
3^{rd} harmonic generation	P_{H3}	–	-90	-85	dBc	25 dBm, 50 Ω, CW mode
Intermodulation Distortion (UMTS Band 1, Band 5)[1]						
2^{nd} order intermodulation	IMD2 low	–	-105	-100	dBm	IMT, US Cell (see Tab. 7)
3^{rd} order intermodulation	IMD3	–	-110	-105	dBm	IMT, US Cell (see Tab. 8)
2^{nd} order intermodulation	IMD2 high	–	-115	-110	dBm	IMT, US Cell (see Tab. 7)
Switching Time						
MIPI to RF time[1]	t_{INT}	–	1.5	2	µs	50 % last SCLK falling edge to 90 % ON, see Fig. 2
Power up settling time[1]	t_{PUP}	–	10	25	µs	After power down mode

[1] On application board without any matching components.

Table 7: IMD2 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	190 (IMD2 low)	-15
			4090 (IMD2 high)	
US Cell	835	20	45 (IMD2 low)	-15
			1715 (IMD2 high)	

Table 8: IMD3 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	1760	-15
US Cell	835	20	790	-15

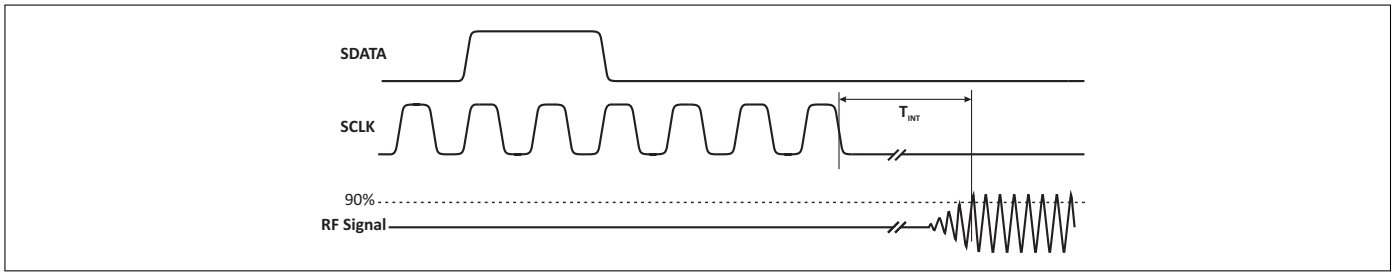


Figure 2: MIPI to RF Time

6 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011.

Table 9: MIPI Features

Feature	Supported	Comment
Register write command sequence	Yes	
Register read command sequence	Yes	
Extended register write command sequence	No	Up to 4 Bytes
Extented register read command sequence	No	Up to 4 Bytes
Register 0 write command sequence	Yes	
Trigger function	Yes	Trigger assignment to each control register is supported
Programmable USID	Yes	3 register command sequence
Status Register	Yes	Register for debugging
Reset	Yes	By VIO, Power Mode and RFFE_STATUS
Group SID	Yes	
SSEL1 and SSEL2 pins	Yes	External pins for changing USID: SSEL1=0 & SSEL2=0 → 1000, SSEL1=0 & SSEL2=1 → 1010, SSEL1=1 & SSEL2=0 → 1001, SSEL1=1 & SSEL2=1 → 1011 To be connected to VIO or GND
Full speed write	Yes	
Half speed read	Yes	
Full speed read	Yes	

Table 10: Startup Behavior

Feature	State	Comment
Power status	ACTIVE	The chip is in active mode after startup. RF-mode is 'All Isolation'
Trigger function	ENABLED	Trigger function is enabled after startup. Trigger function can be disabled via PM_TRIG register.

Table 11: Register Mapping

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x0000	REGISTER_0	7:0	MODE_CTRL	Switch control	00000000	No	Yes	R/W
0x001D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	11010100	No	No	R

Table 11: Register Mapping – Continued from previous page

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x001E	MANUFACTURER_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x001C	PM_TRIG	7:6	PWR_MODE	00: Normal operation 01: Default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved	00	Yes	No	R/W
		5	TRIGGER_MASK_2	If this bit is set, trigger 2 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 2, the data goes directly to the destination register.	0	No	No	
		4	TRIGGER_MASK_1	If this bit is set, trigger 1 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 1, the data goes directly to the destination register.	0	No	No	
		3	TRIGGER_MASK_0	If this bit is set, trigger 0 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 0, the data goes directly to the destination register.	0	No	No	
		2	TRIGGER_2	A write of a one to this bit loads trigger 2's registers.	0	Yes	No	
		1	TRIGGER_1	A write of a one to this bit loads trigger 1's registers.	0	Yes	No	
		0	TRIGGER_0	A write of a one to this bit loads trigger 0's registers.	0	Yes	No	
0x001F	MAN_USID	7:6	SPARE	These are read-only bits that are reserved and yield a value of 0b00 at readback.	00	No	No	R/W
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	See Tab. 9			
0x001A	RFFE_STATUS	7	SOFTWARE RESET	0: Normal operation 1: Software reset	0	No	No	R/W
		6	COMMAND_FRAME_ PARITY_ERR	Command sequence received with parity error - discard command.	0	No	No	R
		5	COMMAND_LENGTH_ERR	Command length error	0			
		4	ADDRESS_FRAME_ PARITY_ERR	Address frame parity error = 1	0			
		3	DATA_FRAME_ PARITY_ERR	Data frame with parity error	0			

Table 11: Register Mapping – Continued from previous page

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
		2	READ_UNUSED_REG	Read command to an invalid address	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_SID	0			
0x001B	GROUP_SID	7:4	RESERVED		0	No	No	R/W
		3:0	GROUP_SID	Group slave ID	0			

Table 12: Modes of Operation (Truth Table, Register_0)

		REGISTER_0 Bits							
State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation	x	x	x	x	x	0	0	0
2	RX01	x	x	x	x	x	0	0	1
3	RX02	x	x	x	x	x	0	1	0
4	RX03	x	x	x	x	x	0	1	1
5	RX04	x	x	x	x	x	1	0	0
6	RX05	x	x	x	x	x	1	0	1

7 Pin Configuration and Function

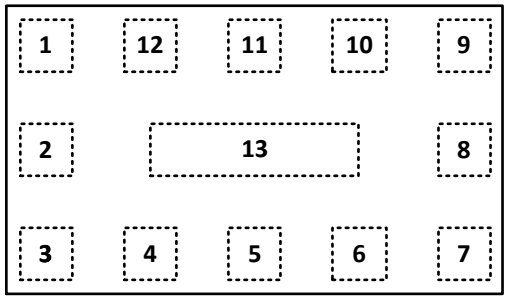


Figure 3: BGS15M2A12 Pin Configuration (top view)

Table 13: Pin Definition and Function

Pin No.	Name	Function
1	SLK	MIPI RFFE clock
2	VIO	MIPI RFFE power supply
3	RX05	RX port 5
4	RX04	RX port 4
5	RX03	RX port 3
6	RX02	RX port 2
7	RX01	RX port 1
8	SSEL1	MIPI USID select port 1 (to be connected to VIO or GND)
9	SSEL2	MIPI USID select port 2 (to be connected to VIO or GND)
10	ANT	Antenna port
11	VDD	Power supply
12	SDATA	MIPI RFFE data
13	GND	RF ground

8 Package Information

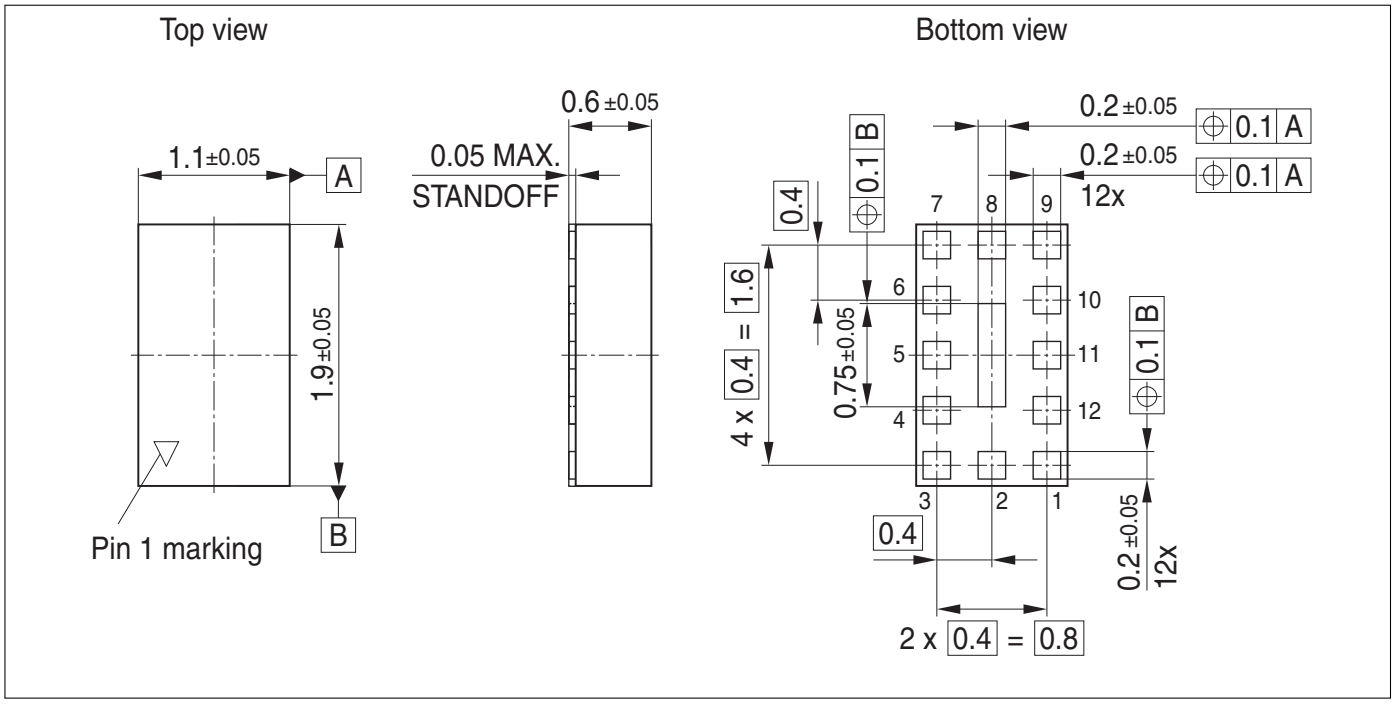


Figure 4: ATSLP-12-5 Package Outline (top, side and bottom views)

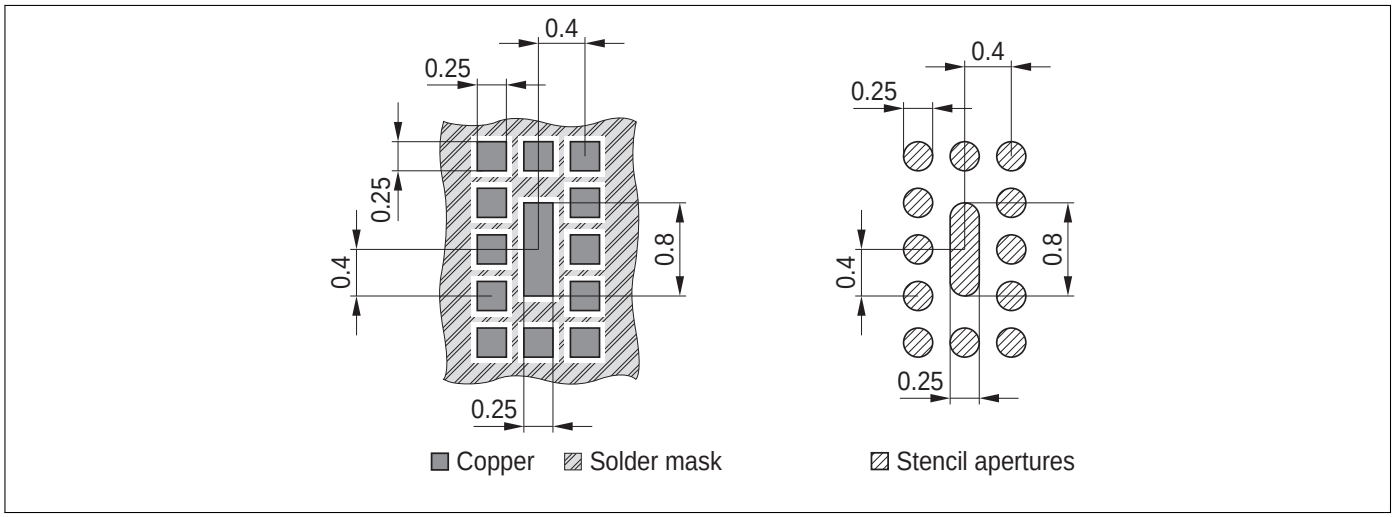


Figure 5: Land Pattern and Stencil Mask

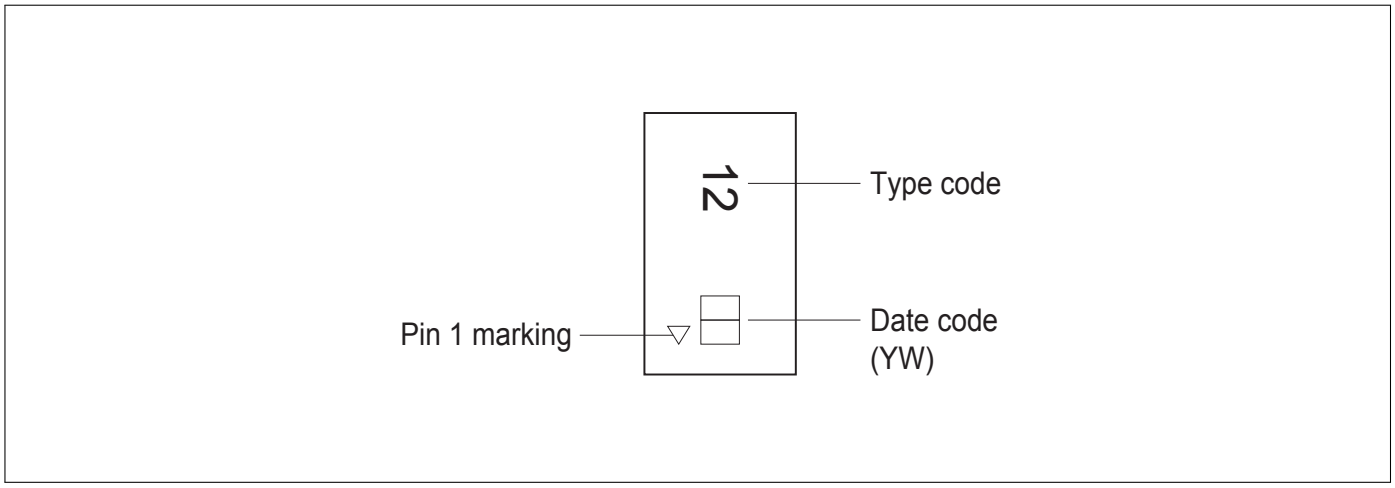


Figure 6: Marking Layout (top view)

9 Packing Information

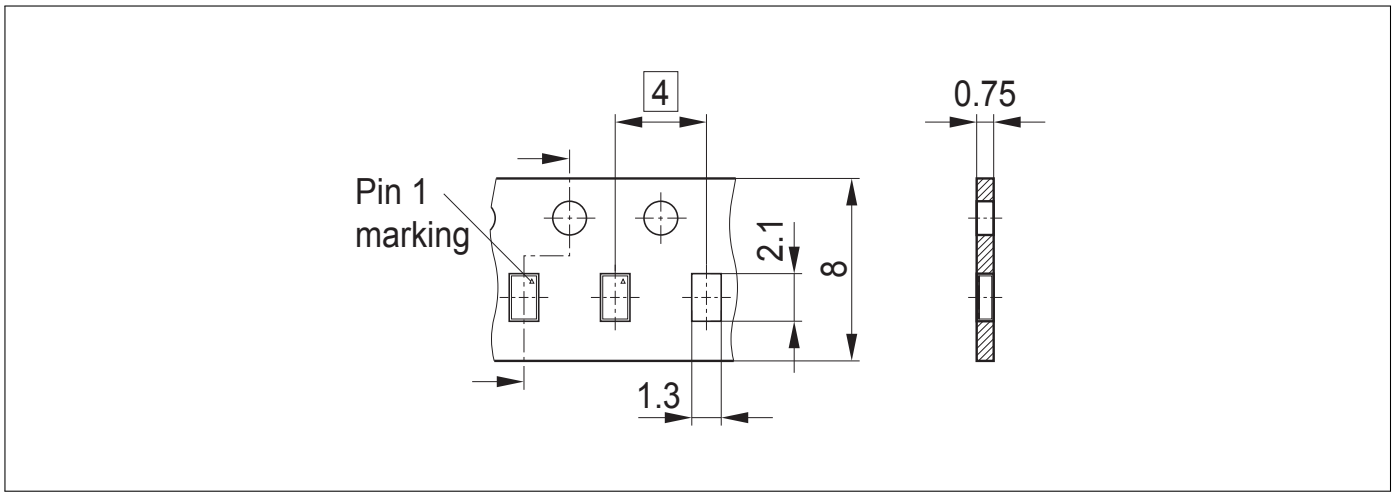


Figure 7: ATSLP-12-5 Carrier Tape

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG